IN THE CLAIMS:

1. (Currently amended) A method of manufacturing a semiconductor apparatus comprising:

forming a first mask material film made of organic insulation film on a film to be processed;

forming a tapered aperture pattern, in which a bottom of said aperture pattern is made narrower than an open side of said aperture pattern, on said first mask material film; and

forming a vertical aperture pattern in said film to be processed by etching said film to be processed using said first mask material film as a mask;

wherein the bottom of the tapered aperture pattern is formed at a desirable micro dimension exceeding capabilities of lithography techniques; and

wherein said forming of the tapered aperture pattern includes cooling the substrate to between about minus 50 degrees Centigrade and about 0 degrees Centigrade.

2. (Previously presented) The method of manufacturing a semiconductor apparatus according to claim 1 further including removing said first mask material film.

3. (Previously presented) The method of manufacturing a semiconductor apparatus according to claim 1 wherein said film to be processed has a step.

4. (Previously presented) The method of manufacturing a semiconductor apparatus according to claim 1 wherein said first mask material film is made of material having a low dielectric constant.

5.-7. (Canceled)

8. (Previously presented) The method of manufacturing a semiconductor apparatus according to claim 1 wherein said first mask material film has a dielectric constant lower than silicon dioxide.

9. (Canceled)

10. (Previously presented) The method of manufacturing a semiconductor apparatus according to claim 1 further comprising forming a second mask material film on the first mask material film.

11 (Currently amended) The method of manufacturing a semiconductor apparatus according to claim ~~10~~ 1 wherein the first mask material film has a heatproof temperature of about 350 degrees Centigrade.

12. (Previously presented) The method of manufacturing a semiconductor apparatus according to claim 10 further comprising forming a resist film on the second mask material film.

13. (Previously presented) The method of manufacturing a semiconductor apparatus according to claim 12 further comprising etching the resist film.

14. (Previously presented) The method of manufacturing a semiconductor apparatus according to claim 13 further comprising etching the second mask material film.

15. (Previously presented) The method of manufacturing a semiconductor apparatus according to claim 3 wherein forming the first mask material film on the film to be processed planarizes an unevenness created by said step.

16. (Canceled)

17. (New) A method of manufacturing a semiconductor apparatus comprising:

forming a first mask material film made of organic insulation film on a film to be processed;

forming a tapered aperture pattern, in which a bottom of said aperture pattern is made narrower than an open side of said aperture pattern, on said first mask material film; and

forming a vertical aperture pattern in said film to be processed by etching said film to be processed using said first mask material film as a mask;

wherein the bottom of the tapered aperture pattern is formed at a desirable micro dimension exceeding capabilities of lithography techniques; and

wherein the first mask material film has a heatproof temperature of about 350 degrees Centigrade.

18. (New) The method of manufacturing a semiconductor apparatus according to claim 17 further including removing said first mask material film.

19. (New) The method of manufacturing a semiconductor apparatus according to claim 17 wherein said first mask material film is made of material having a low dielectric constant.

20. (New) The method of manufacturing a semiconductor apparatus according to claim 17 wherein said first mask material film has a dielectric constant lower than silicon dioxide.

21. (New) The method of manufacturing a semiconductor apparatus according to claim 17 wherein said film to be processed has a step.

22. (New) The method of manufacturing a semiconductor apparatus according to claim 21 wherein forming the first mask material film on the film to be processed planarizes an unevenness created by said step.

23. (New) The method of manufacturing a semiconductor apparatus according to claim 17 further comprising forming a second mask material film on the first mask material film.

24. (New) The method of manufacturing a semiconductor apparatus according to claim 23 further comprising forming a resist film on the second mask material film.

25. (New) The method of manufacturing a semiconductor apparatus according to claim 24 further comprising etching the resist film.

26. (New) The method of manufacturing a semiconductor apparatus according to claim 25 further comprising etching the second mask material film.

27. (New) A method of manufacturing a semiconductor apparatus comprising:

forming a film to be processed having a top surface on a substrate;

forming a first mask material film made of organic insulation film on the film to be processed;

forming a tapered aperture pattern, in which a bottom of said aperture pattern is made narrower than an open side of said aperture pattern, on said first mask material film; and

forming a vertical aperture pattern in said film to be processed by etching said film to be processed using said first mask material film as a mask;

wherein the bottom of the tapered aperture pattern is formed at a desirable micro dimension exceeding capabilities of lithography techniques;

wherein forming the film to be processed on the substrate includes forming at least three successive portions of the film to be processed directly on the substrate, the portions including a first portion having a first thickness, a second portion having a second thickness, which varies between the first thickness and a third thickness to form a step on said top surface, and a third portion having the third thickness; and

wherein forming the first mask material film on the film to be processed planarizes an unevenness created by said step.